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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/749,409	12/28/2000	Herman Kwong	57983.000029	5256	
75	590 03/28/2002	,			
Thomas E. Anderson			EXAMINER		
Hunton & Willi 1900 K Street, I	N.W.		ALCALA, JOSE H		
Washington, DC 20006-1109			ART UNIT	PAPER NUMBER	
			2827		

Please find below and/or attached an Office communication concerning this application or proceeding.

١ ,		Application	No.	Applicant(s)	l,
Office Action Summary		09/749,409		KWONG ET AL.	
		Examiner		Art Unit	
		Jose H Alcal		2841	
Period for F	The MAILING DATE of this commu Reply	nication appears on the c	over sheet with the co	orrespondence address	
THE MA - Extension after SIX - If the per - If NO per - Failure to Any reply	TENED STATUTORY PERIOD F ILING DATE OF THIS COMMUN is of time may be available under the provision (6) MONTHS from the mailing date of this come and for reply specified above is less than thirty (ind for reply is specified above, the maximum is preply within the set or extended period for reply received by the Office later than three months atent term adjustment. See 37 CFR 1.704(b).	IICATION. s of 37 CFR 1.136(a). In no event, munication. days, a reply within the statuto statutory period will apply and will e y will, by statute, cause the applica	however, may a reply be time ry minimum of thirty (30) days xpire SIX (6) MONTHS from t tion to become ABANDONED	ely filed will be considered timely. he mailing date of this communication. 0 (35 U.S.C. § 133).	
	tesponsive to communication(s) f	iled on <u>10 December 20</u>	<u>01</u> .		
2a)□ T	his action is FINAL .	2b)⊠ This action is no	on-final.		
	ince this application is in conditio				
Disposition	losed in accordance with the prac of Claims	ctice under <i>Ex parte Qua</i>	nyle, 1935 C.D. 11, 4	53 O.G. 213.	
•	aim(s) <u>1-30</u> is/are pending in the	. ,			
	Of the above claim(s) <u>1-12 and</u>	<u>25-27</u> is/are withdrawn f	rom consideration.		
·	aim(s) is/are allowed.				
•	aim(s) <u>13-24,28-30</u> is/are rejected	d.			
	aim(s) is/are objected to.				
•	aim(s) are subject to restri	ction and/or election req	uirement.		
Application	•	a Evaminar			
-	e specification is objected to by the drawing(s) filed on 28 Decembe		atad as h) Dahiaatad te	hy the Evaminer	
,	s drawing(s) med on <u>20 Decembe</u> Applicant may not request that any ob	,	,	-	
	e proposed drawing correction file	•			
	approved, corrected drawings are re			, , , , , , , , , , , , , , , , , , ,	
	e oath or declaration is objected t	• • • • • • • • • • • • • • • • • • • •			
Priority und	ler 35 U.S.C. §§ 119 and 120	·			
•	knowledgment is made of a clair	n for foreign priority und	er 35 U.S.C. § 119(a))-(d) or (f).	
a) 🗌	All b) Some * c) None of:		- , ,		
1.		y documents have been	received.		
2.				on No	
3.	application from the Inter	national Bureau (PCT R	ule 17.2(a)).		
	the attached detailed Office acti		•		
	nowledgment is made of a claim				1).
•	☐ The translation of the foreign la knowledgment is made of a claim				
Attachment(s)					
2) Notice o	F References Cited (PTO-892) f Draftsperson's Patent Drawing Review (ion Disclosure Statement(s) (PTO-1449)	(PTO-948) 5		(PTO-413) Paper No(s) Patent Application (PTO-152)	

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DETAILED ACTION

Election/Restrictions

- 1. Applicant's election with traverse of Group II in Paper No. 5 is acknowledged. In response to traversal, the reasoning to distinction has been amended, but the grouping has not been changed. Applicant is required to respond to these new grounds of rejection.
- 2. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process, such as instead of separately forming a first and a second circuit boards, forming an opening in each and then applying an adhesive to join the boards, the product can be made by forming both circuit boards at the same time in an additive process, starting with the ground layers, dielectric, and signal layers of the first circuit board and etching to build the hole, inserting an adhesive and then using a mask to create the holes for the first layer of the second circuit board, and proceeding to deposit the rest of the layers of the circuit board.

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Drawings

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- 3. Figures are improperly crosshatched. All of the parts shown in the section, and only those parts, must be crosshatched. The crosshatching patterns should be selected from those shown on page 600-81 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP 608.02.
- 4. Figure 1A should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
- 5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Reference number 10 is not in Figures 1 and 1A. Reference numbers 100 and 102 are not in Figures 6 and 7. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
- 6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Reference numbers 27a, 27b and 28b from Figure 3A, and 27a, 27b from Figure 3C are not mentioned in the Specification. In addition, reference numbers 46a, 47a, 46b, 47b, and 50a are not mentioned in the Specification. Reference numbers 202, 106a, 106d and 200 are not mentioned in the Specification. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in

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the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "25" has been used to designate both "copper ground place" and "lower surface of PWB" in page 10,line 14. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

- 8. Claim 13 is objected to because of the following informalities: In line 18, the word "the" is misspelled. Appropriate correction is required.
- 9. Claim 21 is objected to because of the following informalities: In line 20, the word "a" needs to be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 112

- The following is a quotation of the second paragraph of 35 U.S.C. 112:
 The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 11. Claims 14,19,21,22,24 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the exact location of the via in the printed boards, it is not clear how the via can be inside of the opening. Is the opening completely filled with a material and having a via inside, or is the via just a way to label the opening.

Claim 19 recites the limitation "the first signal conductor" in line 1. In addition, the claim recites the limitation "the second signal conductor" in line 2, and the limitation "the ground plane layers" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the exact location of the third signal conducting means in the first circuit board, and the exact location of the fourth signal conducting means in the second circuit board.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 13-24,28-30 rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art in view of Swamy (US Patent No. 5,576,519) and further in view of Daigle et al. (US Patent No. 5,046,238). As best understood by the examiner:

Regarding Claim 13, Applicant's Admitted Prior Art teaches circuit boards (Reference number 11) having a signal conducting means formed therein (Reference number 26), the signal conducting means being shielded by an electrically conductive shield (Reference number 28), the electrically conductive shield having an opening (Reference Number 30) formed therein so as to expose the signal conducting means in the circuit board.

Applicant's Admitted Prior Art fails to teach an electrically conductive adhesive, solder paste, or interposer/elastomer device applied surrounding at least one of the openings and within at least one of the openings; wherein a first circuit board and a second circuit board are electrically interconnected by the electrically conductive adhesive, solder paste, or interposer/elastomer device such that the first opening and the second opening are aligned and a signal propagating along the first signal conducting means is electrically interconnected to the second signal conducting means.

Daigle et al. teaches an electrically conductive adhesive, solder paste, or interposer/elastomer device (Reference Number 21) within at least one of the openings; wherein a first circuit board (Reference number X1) and a second circuit board (Reference number X2) are electrically interconnected by the electrically conductive

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adhesive, solder paste, or interposer/elastomer device such that the first opening and the second opening are aligned (See Figure 6) and a signal propagating along the first signal conducting means is electrically interconnected to the second signal conducting means.

Swamy teaches an electrically conductive adhesive, solder paste, or interposer/elastomer device (Reference Number 106) applied surrounding at least one of the openings; wherein a first circuit board (Reference number MLB #1) and a second circuit board (Reference number MLB #2) are electrically interconnected by the electrically conductive adhesive, solder paste, or interposer/elastomer device such that the first opening and the second opening are aligned (See Figure 3) and a signal propagating along the first signal conducting means is electrically interconnected to the second signal conducting means.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Applicant's Admitted Prior Art, Swamy and Daigle in order to interconnect two of the circuit boards using an electrically conductive adhesive, solder paste, or interposer/elastomer device applied surrounding at least one of the openings and within at least one of the openings, such that the first opening and the second opening are aligned and a signal propagating along the first signal conducting means is electrically interconnected to the second signal conducting means. Thus, improving integration by allowing stacking of a large quantity of circuit boards together, and improving the conduction from one board to the other by providing more electrically conductive contact points between them.

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Regarding Claim 14, the combination of Applicant's Admitted Prior Art, Swamy and Daigle teaches that there is electrically conductive adhesive or solder paste within a first via located within the first opening and within a second via located within the second opening.

Regarding Claim 15, the combination of Applicant's Admitted Prior Art, Swamy and Daigle fails to explicitly teach that the first signal conducting means comprises a pair of signal conductors and the second signal conducting means comprises a pair of signal conductors. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the conducting means of both circuit boards comprising more than one signal conductors, in order to improve the signal transmission properties of the circuit board. In addition, it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. See St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Regarding Claim 16, the combination of Applicant's Admitted Prior Art, Swamy and Daigle teaches that the first signal conducting means and the second signal conducting means each comprise a single conductor.

Regarding Claim 17, the combination of Applicant's Admitted Prior Art, Swamy and Daigle teaches that the first circuit board and the second circuit board are multilayer circuit boards (See Figure 3 of Swamy), wherein the first electrically conductive shield and the second electrically conductive shield are respective electrically conductive layers of the first circuit board and the second circuit board (Suggested from Figure 2A of Applicant's admitted Prior Art).

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Regarding Claim 18, the combination of Applicant's Admitted Prior Art, Swamy and Daigle suggests that the first electrically conductive shield and the second electrically conductive shield can be formed by respective ground plane layers of the first circuit board and the second circuit board (See the Swamy reference, Figure 2).

Regarding Claim 19, the combination of Applicant's Admitted Prior Art, Swamy and Daigle suggests that the first signal conductor and the second signal conductor are formed on respective signal layers of the first circuit board and the second circuit board, wherein the signal layers are disposed beneath the ground plane layers in the first circuit board and the second circuit board (Applicant's Admitted Prior Art in Figure 2A, teaches that the signal conductor is disposed beneath the electrically conductive shield that can be a ground plane layer.

Regarding Claim 20, the combination of Applicant's Admitted Prior Art, Swamy and Daigle teaches all the structural limitations of the invention as stated supra, thus it inherently has a signal that carries data at a rate on the order of 1 Gb/s and above.

Regarding Claim 21, the combination of Applicant's Admitted Prior Art, Swamy and Daigle fails to explicitly teach that the first circuit board has a third signal conducting means formed therein, wherein the third signal conducting means is shielded by a third electrically conductive shield, wherein a third opening is formed in the third electrically conductive shield so as to expose the third signal conducting means in the first circuit board; wherein the second circuit board has a fourth signal conducting means formed therein, wherein the fourth signal conducting means is shielded by a fourth electrically conductive shield, wherein a fourth opening is formed in the fourth electrically

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conductive shield so as to expose the fourth signal conducting means in the second circuit board; wherein an electrically conductive adhesive, solder paste, or interposer/elastomer device is applied around at least one of the third and fourth openings and within at least one of the third and fourth openings; and wherein the first circuit board and the second circuit board are positioned such that the third opening and the fourth opening are aligned and another signal propagating along the third signal conducting mans is electrically connected to the fourth signal conducting means.

Applicant's Admitted Prior Art teaches in Fig 2A that the circuit boards have two signal conducting means each, so if two of those circuit boards are joined one to the other as stated supra on the combination of the three references, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make more conducting means on each circuit boards, in order to improve the signal transmission properties of the circuit boards. In addition, it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. See St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Regarding Claim 22, the combination of Applicant's Admitted Prior Art, Swamy and Daigle fails to explicitly say that the third electrically conductive shield can be electrically connected to the first electrically conductive shield, and that the fourth electrically conductive shield is electrically connected to the second electrically conductive shield. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings in order to have the third electrically conductive shield can be electrically connected to the first electrically

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conductive shield, and that the fourth electrically conductive shield is electrically connected to the second electrically conductive shield, since the pattern in which the electrically conductive shields are connected between the two circuit boards will not affect the proper function of the device.

Regarding Claim 22, the combination of Applicant's Admitted Prior Art, Swamy and Daigle teaches all of the structural limitations of claim 13 as stated supra. The limitations that the first circuit board is a motherboard, wherein the second circuit board is a daughterboard, are intended use limitations and it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. SeeEx parte Masham, 2 USPQ 2d 1647 (1987).

Regarding Claim 24, the combination of Applicant's Admitted Prior Art, Swamy and Daigle teaches that the daughterboard (one of the circuit boards) is formed at least partially of a dielectric that can be a flexible material. The limitation that: "to allow angular mating with the motherboard" is an intended use limitation, and it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. See Ex parte Masham, 2 USPQ 2d 1647 (1987).

Regarding Claim 28, Applicant's Admitted Prior Art teaches circuit boards

(Reference number 11) having a signal conducting means (Reference number 26)

formed therein, the signal conducting means being shielded by a electrically conductive

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shield (Reference number 28), the electrically conductive shield having an opening (Reference Number 30) formed therein so as to expose the signal conducting means in the circuit board;

Applicant's Admitted Prior Art fails to teach an electrically conductive adhesive, solder paste, or interposer/elastomer device applied surrounding at least one of the openings and within at least one of the openings; wherein a first circuit board and a second circuit board are electrically interconnected by the electrically conductive adhesive, solder paste, or interposer/elastomer device such that the first opening and the second opening are aligned and a signal propagating along the first signal conducting means is electrically interconnected to the second signal conducting means.

Daigle et al. teaches an electrically conductive adhesive, solder paste, or interposer/elastomer device (Reference Number 21) within at least one of the openings; wherein a first circuit board (Reference number X1) and a second circuit board (Reference number X2) are electrically interconnected by the electrically conductive adhesive, solder paste, or interposer/elastomer device such that the first opening and the second opening are aligned (See Figure 6) and a signal propagating along the first signal conducting means is electrically interconnected to the second signal conducting means.

Swamy teaches an electrically conductive adhesive, solder paste, or interposer/elastomer device (Reference Number 106) applied surrounding at least one of the openings; wherein a first circuit board (Reference number MLB #1) and a second circuit board (Reference number MLB #2) are electrically interconnected by the

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electrically conductive adhesive, solder paste, or interposer/elastomer device such that the first opening and the second opening are aligned (See Figure 3) and a signal propagating along the first signal conducting means is electrically interconnected to the second signal conducting means.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Applicant's Admitted Prior Art, Swamy and Daigle in order to interconnect two of the circuit boards using an electrically conductive adhesive, solder paste, or interposer/elastomer device applied surrounding at least one of the openings and within at least one of the openings, such that the first opening and the second opening are aligned and a signal propagating along the first signal conducting means is electrically interconnected to the second signal conducting means. Thus, improving integration by allowing stacking of a large quantity of circuit boards together, and improving the conduction from one board to the other by providing more electrically conductive contact points between them.

Regarding Claim 29, the combination of Applicant's Admitted Prior Art, Swamy and Daigle fails to explicitly teach that the first signal conducting means comprises a pair of signal conductors and the second signal conducting means comprises a pair of signal conductors and that each conductor of the first pair is connected with a conductor of the second pair for transmission of two signals between the first pair and the second pair.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the conducting means of both circuit boards

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comprising more than one signal conductors and to ensure that each conductor of the first pair is connected with a conductor of the second pair for transmission of two signals between the first pair and the second pair, in order to improve the signal transmission properties of the circuit board. In addition, it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. See St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Regarding Claim 30, the combination of Applicant's Admitted Prior Art, Swamy and Daigle teaches that the first signal conducting means and the second signal conducting means each comprise a single conductor.

Conclusion

- 14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references teach some of the elements of the instant claimed invention: Basavanhally et al. (US Patent No. 5,225,966), Asada (US Patent No. 6,239,496), Okano et al. (US Patent No. 5,679,928), Shimada et al. (US Patent No. 6,353,1898) and Jiang et al. (US Patent No. 6,163,957).
- 15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

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- 16. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.
- 17. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA March 24, 2002

Klunes Annay Examin

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